1. A sequential circuit has two inputs (X1, X2) and one output (Z). The output remains a constant value unless one of the following input sequences occurs:

a. The input sequence X1 X2 = 01, 11 causes the output to become ‘0’.

b. The input sequence X1 X2 = 10, 11 causes the output to become ‘1’.

c. The input sequence X1 X2 = 10, 01 causes the output to change value.

The notation X1 X2 = 10, 01 means X1 = 0, X2 = 1 followed by X1 = 1, X2 = 1.

Derive a Moore state graph and state table for the circuit.

Answer.) With respect to the above input sequences and condition of Z mentioned, a state graph for the sequential circuit has to be derived.

To start off, for six inputs (01,11,10,11,10,01) six states can be defined.

|  |  |  |
| --- | --- | --- |
| Previous Input (X1 X2) | Output (Z) | State Designation |
| 11 or 00 | 0 | S0 |
| 11 or 00 | 1 | S1 |
| 01 | 0 | S2 |
| 01 | 1 | S3 |
| 10 | 0 | S4 |
| 10 | 1 | S5 |

The input can either be 11 **or** 00 because neither input will start a changed sequence in output. From the input 00 or 11, the output can be in either of two basic states – 1 or 0. The output will remain latched unless an input aside from 00/11 is given.

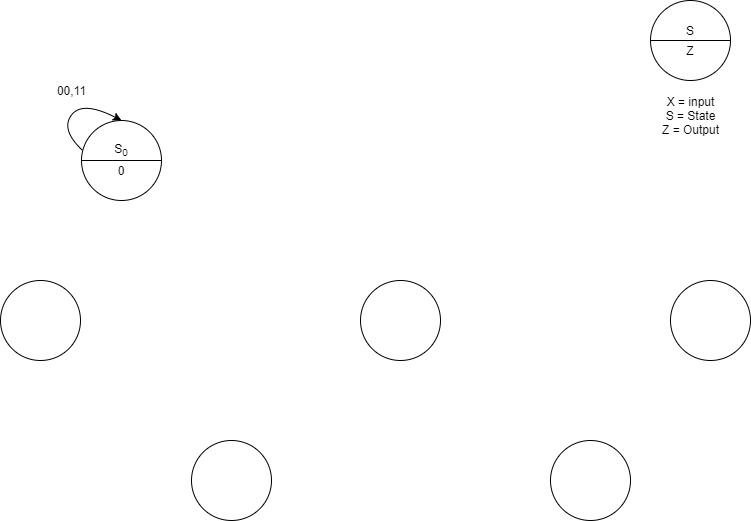
Now, a state table can be made: -

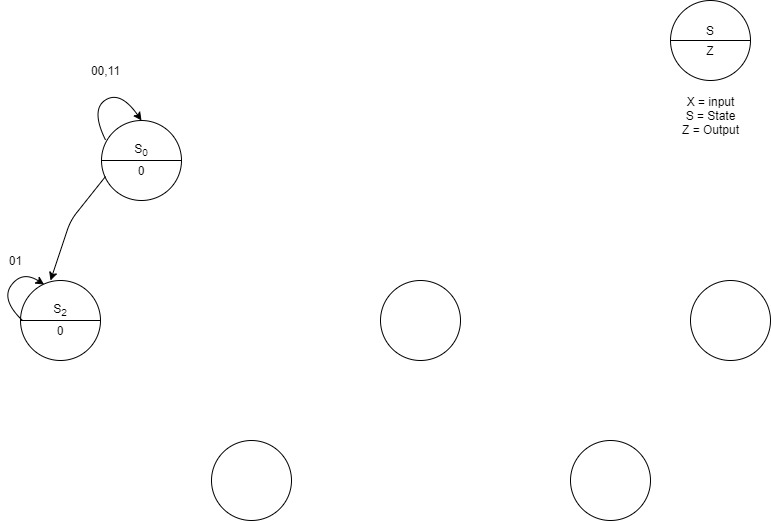
Next State

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| State Designation | Previous State | Output (Z) | 00 | 01 | 11 | 10 |
| S0 | 11 or 00 | 0 | 0 | 0 | 0 | 0 |
| S1 | 11 or 00 | 1 | 1 | 1 | 1 | 1 |
| S2 | 01 | 0 | 0 | 0 | 0 | 0 |
| S3 | 01 | 1 | 1 | 1 | 0 | 1 |
| S4 | 10 | 0 | 0 | 1 | 1 | 0 |
| S5 | 10 | 1 | 1 | 0 | 1 | 0 |

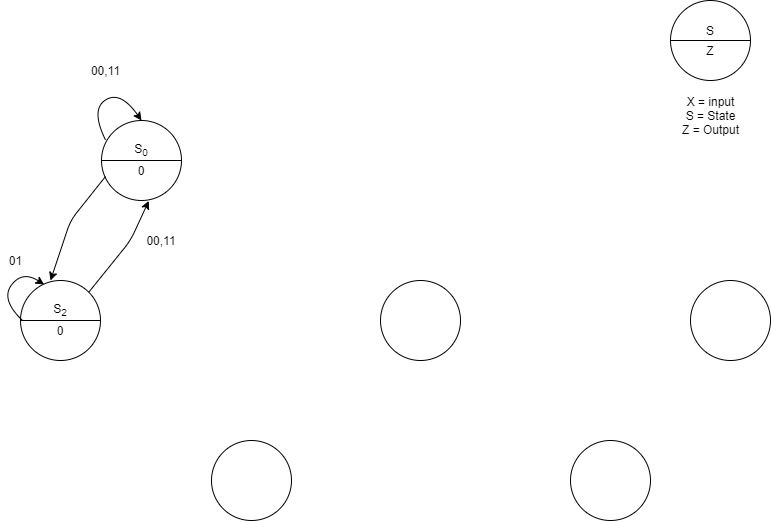
**S0 ROW**

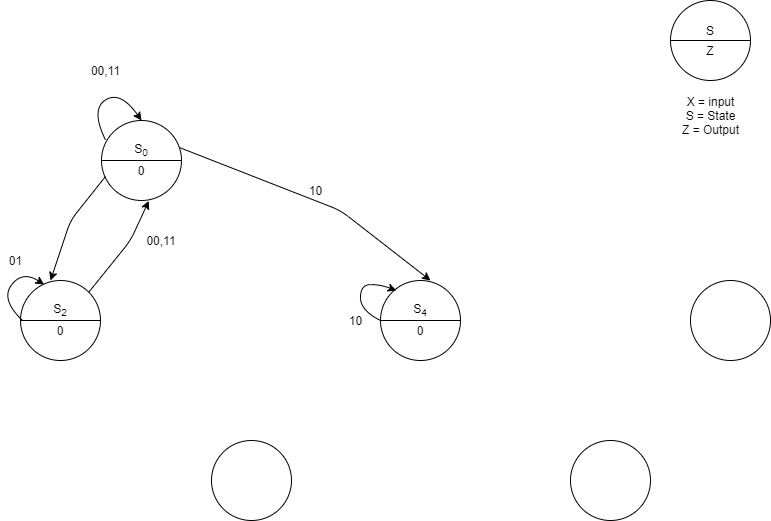
When 00 is received then the input sequence is 00,00, we go back to the same state (S0).



When 01 is received, then the input sequence is 00,01 we will move to S2 (output will be 0).

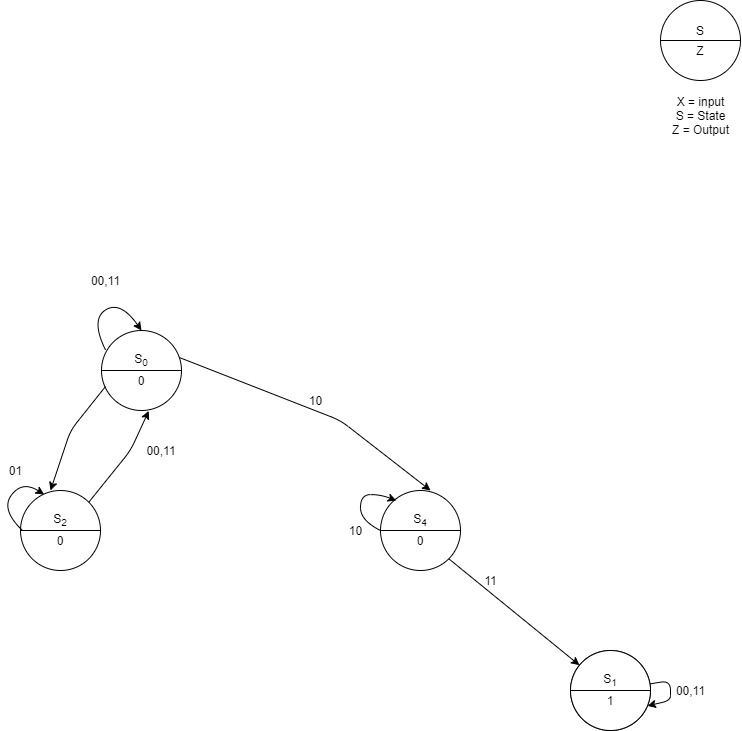
When 11 is received, then the input sequence is 00,11 and we go back to S0 (output is 0).



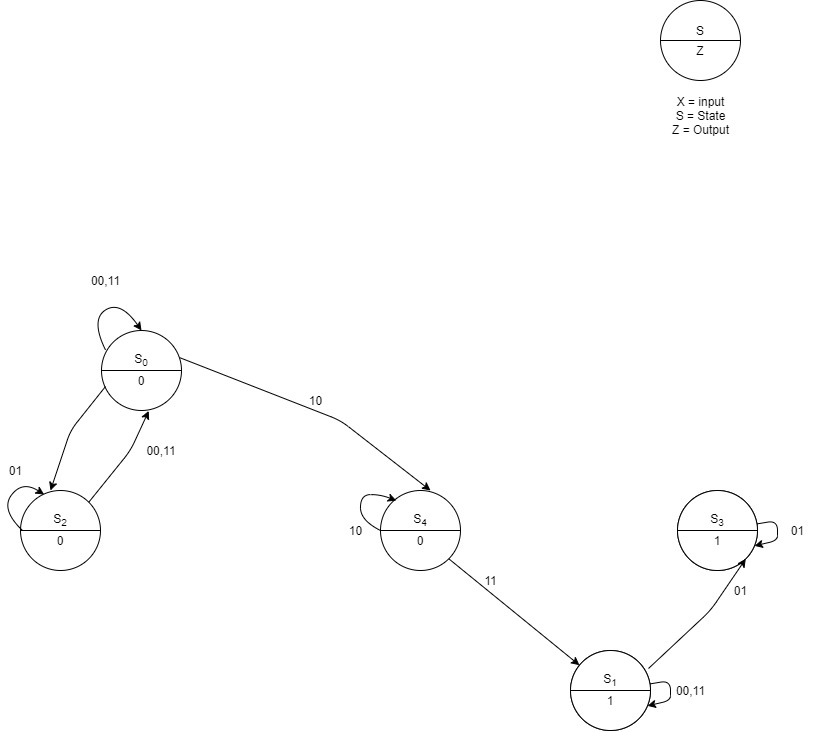
When 10 is received, the input sequence is 00,10 and so we go to S4 (output is 0).

**S1 ROW**

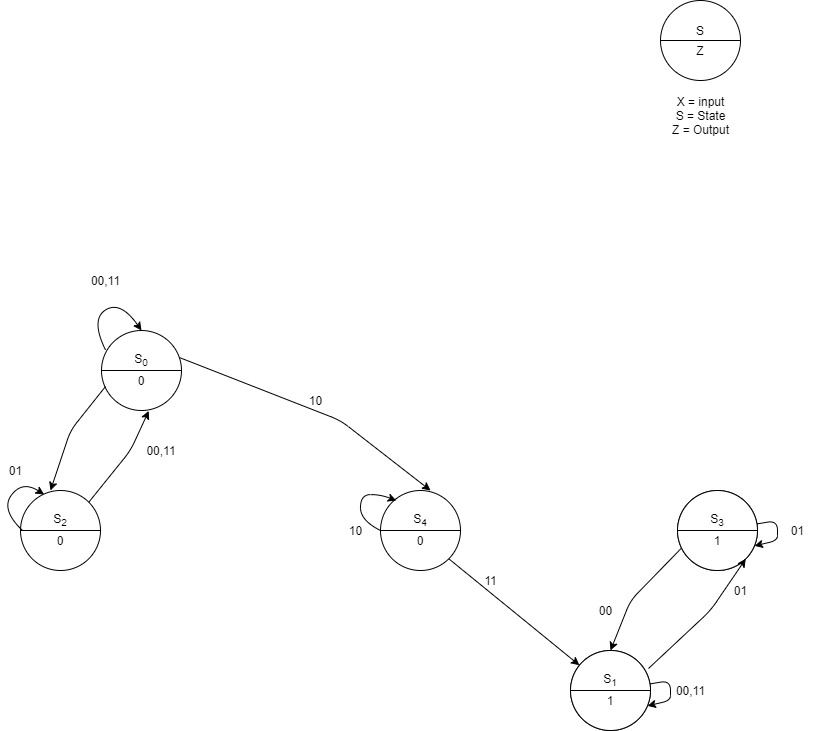
Moving on, when 00 is received, the input sequence is 00,11 and so we go to S1 and the output will now change to 1.



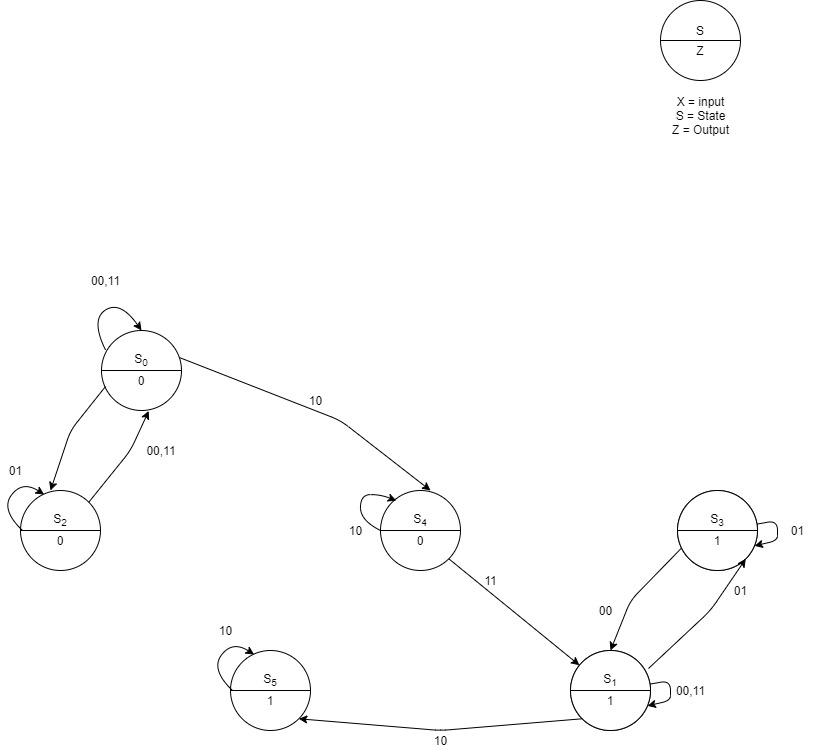
When 01 is received, the input sequence will be 11,01 and we will move to S3 (output will be 1).



When 11 is received, the input sequence becomes 11,11 and so we go back to S1. (output will be 1).

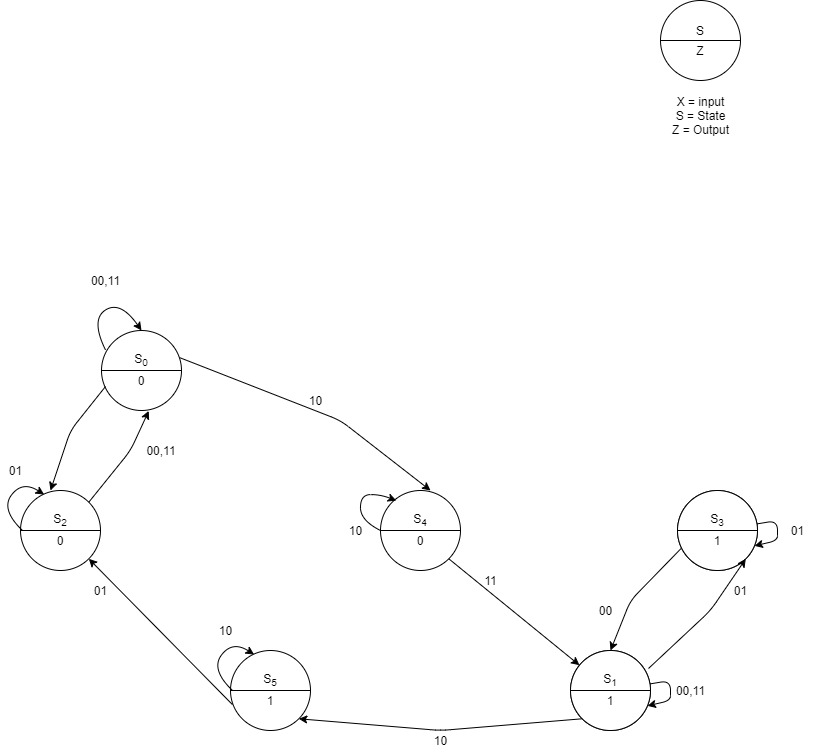


When 10 is received, the input sequence is 11, 10 and we move to S5 (output will be 1).



**S2 ROW**

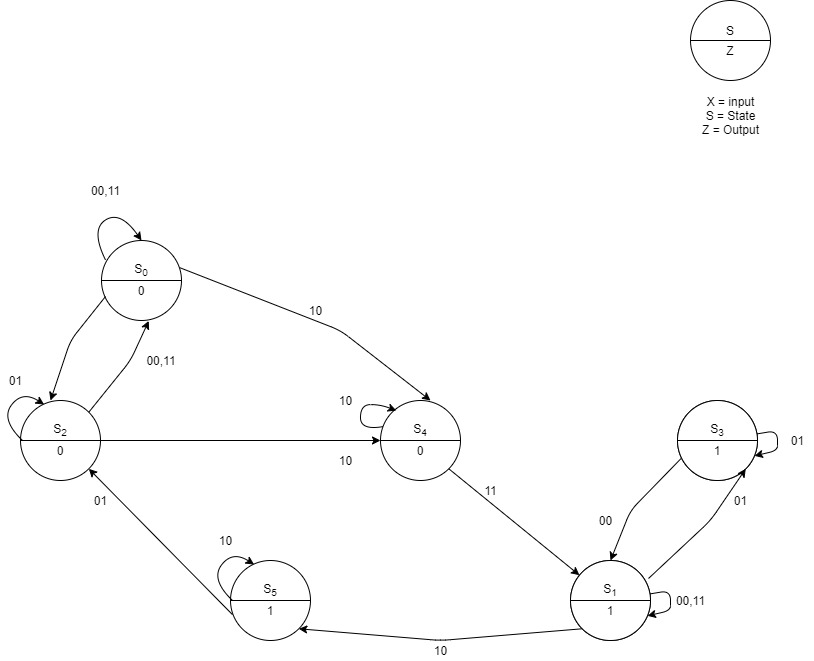
When 00 is received, the input sequence is 01,00 and we move to S0 because the output will be 0.



When 01 is received, the input sequence is 01, 01 and we move to S2 (output will be 0).

When 11 is received, the input sequence becomes 01, 11 and we go to S0 (output will be 0).

When 10 is received, the input sequence is 01, 10 and we go to S4 (output will be 0).

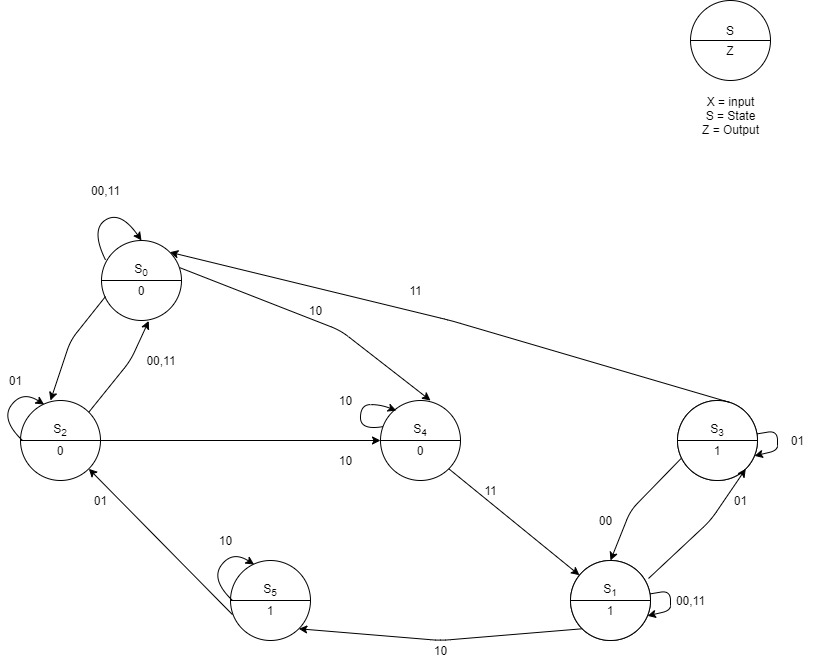


**S3 ROW**

When 00 is received, the input sequence is 01,00 and we go to S1 (output will be 1).

When 01 is received, the input sequence is 01, 01 and we go to S3 (output will be 1).

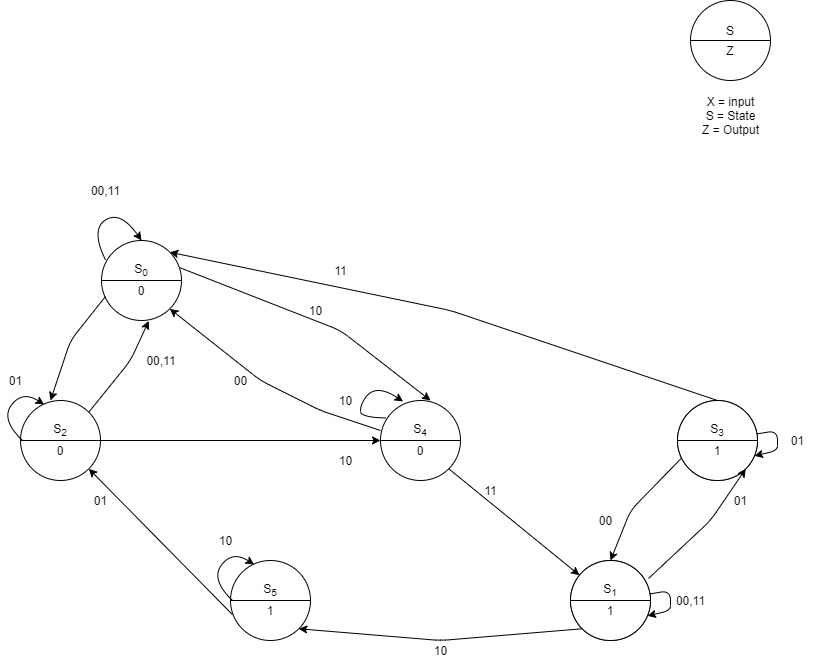
When 11 is received, the input sequence is 01, 11 and we go to S0 (output will be 0).



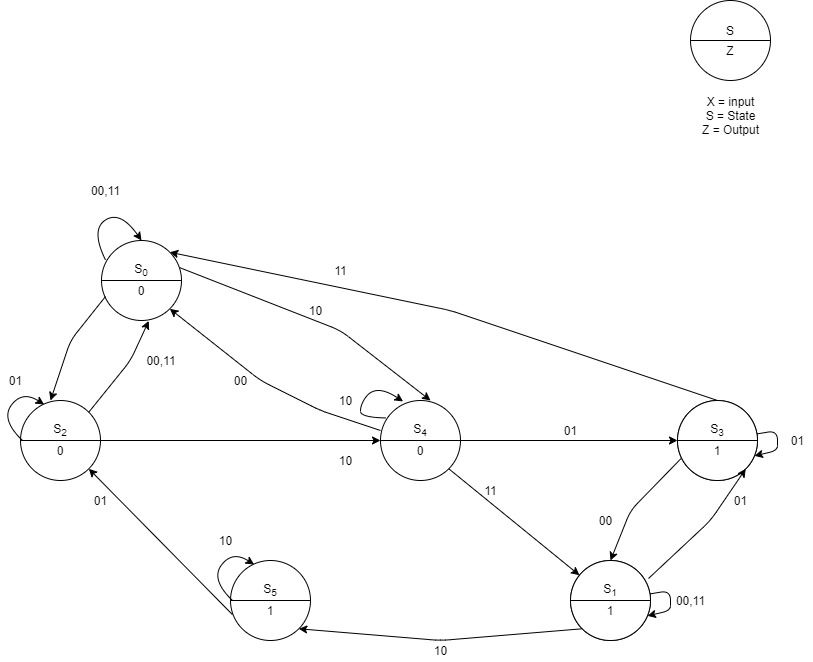
When 10 is received, the input sequence is 01, 10 and we move to S5 (output will be 1).

**S4 ROW**

When 00 is received, the input sequence is 10, 00 and we go to S0 (output will be 0).



When 01 is received, the input sequence is 10, 01 and we move to S3 (output will be 1).

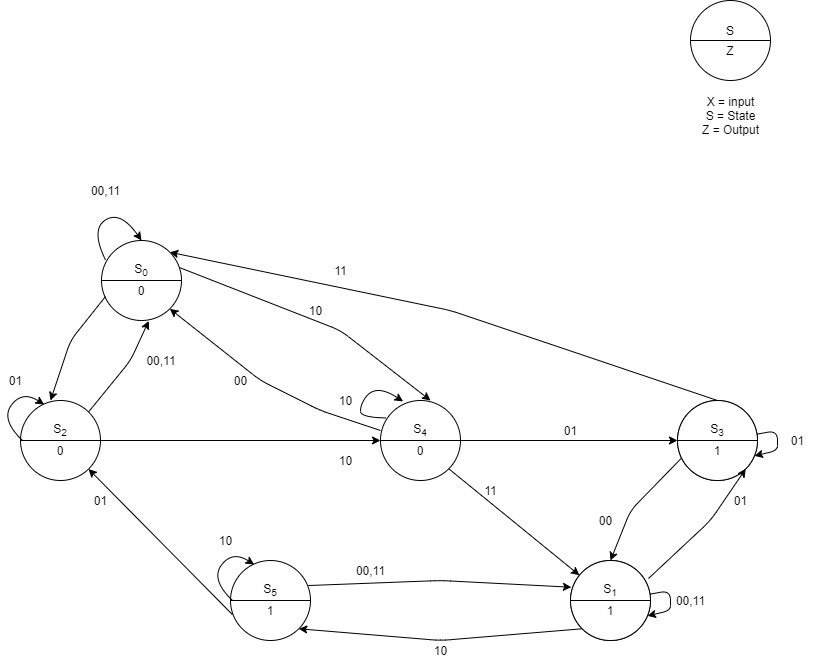


When 11 is received, the input sequence is 10, 11 and we move to S1 rather than moving to S0 because the output is 1.

When 10 is received, the input sequence is 10,10 and we move to S4 (output will be 0).

**S5 ROW**

When 00 is received, the input sequence is 10, 00 and we go to S1



When 01 is received, the input sequence is 10, 01 and we move to S2

When 11 is received, the input sequence is 10, 11 and we move to S1

When 10 is received, the input sequence is 10,10 and we move to S5

A simpler version of the state table: -

Next State

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Previous Input | Output (Z) | 00 | 01 | 11 | 10 |
| S0 | 0 | S0 | S2 | S0 | S4 |
| S1 | 1 | S1 | S3 | S1 | S5 |
| S2 | 0 | S0 | S2 | S0 | S4 |
| S3 | 1 | S1 | S3 | S0 | S5 |
| S4 | 0 | S0 | S3 | S1 | S4 |
| S5 | 1 | S1 | S2 | S1 | S5 |

At last, the final State Graph: -

